In the Claims

Applicant has submitted a new complete claim set showing marked up claims with insertions indicated by underlining and deletions indicated by strikeouts and/or double bracketing.

1. (Original) A measuring circuit for determining a characteristic of the impedance of a complex impedance element for facilitating characterization of the impedance thereof, the measuring circuit being implemented on a single chip and comprising:

a signal generating circuit for generating an analog stimulus signal of selectable frequency for applying to the complex impedance element,

a first receiving circuit for receiving an analog response signal from the complex impedance element in response to the stimulus signal, and for outputting a first output signal indicative of the characteristic of the impedance of the complex impedance element for use in characterization of the impedance of the complex impedance element.

2. (Currently amended) A measuring circuit as claimed in Claim 1 or claim 15 in which the first receiving circuit is operable for outputting the first output signal to be indicative of one of a phase shift and an amplitude change of the stimulus signal caused by the complex impedance element.

3. (Original) A measuring circuit as claimed in Claim 2 in which the first receiving circuit is operable for selectively and alternately outputting the first output signal to be indicative of one of the phase shift and the amplitude change of the stimulus signal caused by the complex impedance element.

4. (Original) A measuring circuit as claimed in Claim 2 in which the first receiving circuit comprises a selectable first converting circuit for converting the analog response signal from the complex impedance element to a voltage signal suitable for comparison with the stimulus signal.

5. (Original) A measuring circuit as claimed in Claim 4 in which the first converting circuit comprises a selectable first root-mean-square (RMS) to DC voltage converter for converting the analog response signal from the complex impedance element to a DC voltage level corresponding to the RMS voltage value of the analog response signal.

6. (Currently amended) A measuring circuit as claimed in Claim 1 or claim 15 in which the first receiving circuit comprises a current to voltage converting circuit for converting the analog response signal to an analog voltage signal.

7. (Currently amended) A measuring circuit as claimed in Claim 1 or claim 15 in which the first receiving circuit comprises a first analog-to-digital converter for converting the analog response signal from the complex impedance element to a digital signal for providing the first output signal as a digital signal.

8. (Original) A measuring circuit as claimed in Claim 7 in which the first receiving circuit comprises a first storing means for storing the first output signal in digital form.

9. (Currently amended) A measuring circuit as claimed in Claim 1 or claim 15 in which a calibration circuit is provided on the chip for determining a calibration coefficient for calibrating the first receiving circuit, the calibration circuit comprising a coefficient storing means for storing the calibration coefficient.

10. (Original) A measuring circuit as claimed in Claim 9 in which a compensating circuit is provided on the chip for selectively applying the calibration coefficient to the first output signal for correcting the first output signal for errors introduced to the response signal by the first receiving circuit.

11. (Original) A measuring circuit as claimed in Claim 9 in which a first coupling circuit is provided on the chip for selectively applying the stimulus signal to the first receiving circuit for calibration thereof.

12. (Original) A measuring circuit as claimed in Claim 1 in which a second receiving circuit is provided on the chip for receiving the analog stimulus signal and for outputting a second output signal representative of the stimulus signal for comparison with the first output signal for facilitating a determination of the characteristic of the impedance of the complex impedance element.

13. (Original) A measuring circuit as claimed in Claim 12 in which the second receiving circuit comprises a second analog-to-digital converter for converting the analog stimulus signal to a digital signal for providing the second output signal as a digital signal.

14. (Original) A measuring circuit as claimed in Claim 13 in which the second receiving circuit comprises a second storing means for storing the second output signal in digital form.

15. (Currently amended) A measuring circuit as claimed in Claim 12 in which the second ~~converting~~ receiving circuit comprises a selectable second RMS to DC voltage converter for converting the analog stimulus signal to a DC signal of voltage level corresponding to the RMS value of the analog stimulus signal.

16. (Original) A measuring circuit as claimed in Claim 12 in which the second receiving circuit comprises an input signal switching circuit for selectively and alternately applying one of the analog stimulus signal and a signal from a temperature sensor to the second receiving circuit.

17. (Original) A measuring circuit as claimed in Claim 16 in which the temperature sensor is provided on the chip.

18. (Original) A measuring circuit as claimed in Claim 12 in which a second coupling circuit is provided on the chip for selectively applying the analog stimulus signal to the second receiving circuit.

19. (Original) A measuring circuit as claimed in Claim 12 in which a signal processing circuit is provided on the chip for processing one or both of the first output signal and second output signal, and for outputting a third output signal resulting from the processing of the one or both of the first and second output signals.

20. (Currently amended) A measuring circuit as claimed in Claim 1 or claim 15 in which the signal generating circuit comprises a signal conditioning circuit for setting one of the voltage level and the current level of the stimulus signal.

21. (Currently amended) A measuring circuit as claimed in Claim 1 or claim 15 in which the signal generating circuit comprises a direct digital synthesis frequency signal generator for generating the stimulus signal.

22. (Original) A measuring circuit as claimed in Claim 21 in which the direct digital synthesis frequency signal generator comprises:

a phase accumulator comprising a counter for incrementing or decrementing its count by a frequency determining digital word to or from a predetermined maximum count value in response to each cycle of a clock signal,

a phase-to-amplitude converter for converting count values from the phase accumulator to digital words representative of amplitude values of the stimulus signal, and

a digital-to-analog converter for converting the digital words from the phase-to-amplitude converter to the stimulus signal.

23. (Original) A measuring circuit as claimed in Claim 22 in which the phase-to-amplitude converter comprises a look-up table with the digital words representative of the amplitude values of the stimulus signal cross-referenced with count values from zero to the predetermined maximum count value outputted by the phase accumulator.

24. (Original) A measuring circuit as claimed in Claim 22 in which the stimulus signal generated by the signal generator is of sinusoidal waveform.

25. (Original) A measuring circuit as claimed in Claim 22 in which a first bypass circuit is provided for applying the count values from the phase accumulator directly to the digital-to-analog converter so that the stimulus signal provided from the digital-to-analog converter is of triangular waveform.

26. (Original) A measuring circuit as claimed in Claim 22 in which a second bypass circuit bypasses the digital-to-analog converter for applying the count values from the phase accumulator to a comparator for comparing the most significant bit of the count values with a reference value for providing the stimulus signal as a square waveform.

27. (Original) A measuring circuit as claimed in Claim 22 in which the direct digital synthesis frequency signal generator comprises an adder for summing a phase offset digital word to each count value outputted by the phase accumulator for offsetting the phase of the stimulus signal by a predetermined offset.

28. (Original) A measuring circuit as claimed in Claim 27 in which the phase offset digital word is selectable for selecting the phase offset of the stimulus signal.

29. (Original) A measuring circuit as claimed in Claim 22 in which the frequency determining digital word is selectable for selecting the frequency of the stimulus signal.

30. (Currently amended) A measuring circuit as claimed in Claim 1 or claim 15 in which the measuring circuit is implemented as an integrated circuit.

31. (Original) A method for determining a characteristic of the impedance of a complex impedance element for facilitating characterization of the impedance thereof, the method comprising the steps of:

providing a signal generating circuit on a single chip for generating an analog stimulus signal of selectable frequency for applying to the complex impedance element,

providing a first receiving circuit on the single chip for receiving an analog response signal from the complex impedance element in response to the stimulus signal and for outputting a first output signal indicative of the characteristic of the impedance of the complex impedance element for use in characterization of the impedance of the complex impedance element,

operating the signal generating circuit for applying the stimulus signal to the complex impedance element,

applying an analog response signal from the complex impedance element, responsive to the stimulus signal, to the first receiving circuit, and

operating the first receiving circuit for outputting the first output signal indicative of the characteristic of the impedance of the complex impedance element.

32. (Original) A method as claimed in Claim 31 in which the first receiving circuit is operated for selectively and alternately outputting the first output signal to be indicative of one of a phase shift and an amplitude change of the stimulus signal caused by the complex impedance element.

33. (Original) A method as claimed in Claim 31 in which the response signal from the complex impedance element is converted in the first receiving circuit to a voltage signal suitable for comparison with the stimulus signal.

34. (Original) A method as claimed in Claim 33 in which the response signal from the complex impedance element is converted in the first receiving circuit to a DC signal of voltage level corresponding to the RMS voltage value of the analog response signal.

35. (Original) A method as claimed in Claim 31 in which the analog response signal from the complex impedance circuit is converted to a digital signal in the first receiving circuit for providing the first output signal as a digital signal.

36. (Original) A method as claimed in Claim 31 in which the method comprises the further step of fabricating a second receiving circuit on the single chip for receiving the analog stimulus signal and for outputting a second output signal representative of the stimulus signal for comparison with the first output signal for facilitating a determination of the characteristic of the impedance of the complex impedance element.

37. (Original) A method as claimed in Claim 36 in which the analog stimulus signal is converted to a digital signal in the second receiving circuit for providing the second output signal as a digital signal.

38. (Original) A method as claimed in Claim 36 in which the analog stimulus signal is converted in the second receiving circuit to a DC signal of voltage level corresponding to the RMS value of the analog stimulus signal.

39. (Original) A method as claimed in Claim 31 in which the signal generating circuit is provided as a direct digital synthesis frequency signal generator.